1. A method for fabricating multilevel metal interconnections having low dielectric constant insulators on a substrate comprising the steps of:

providing a semiconductor substrate having semiconductor devices in and on said substrate;

depositing a first insulating layer over said devices, and further having contact openings in said first insulating layer for electrical contacts to said devices;

forming a metal barrier layer on said insulating layer and in said contact openings;

depositing a first conductive layer for contacting said contact openings;

patterning said first conductive layer and said metal barrier layer to form first metal lines as interconnections for said devices;

coating a layer of low dielectric constant insulating material on and in between said patterned interconnect metal lines;

curing the low dielectric constant material;

depositing thin layer of an adhesion promoter and stabilizing material on the low dielectric constant material;

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depositing a silicon oxide cap layer on the adhesion promoter and over the low dielectric constant material;

planarizing the oxide surface with chemical mechanical polish (CMP);

defining via openings and etching to open electrical contacts to the underlying interconnect metal;

depositing conductive metal over the via openings;

removing the excess said conductive metal by CMP;

patterning of said conductive layer to form the next level of metal interconnections.

2. The method of claim 1, wherein said low dielectric constant material is SOD, spun on dielectric, especially organic compounds and is coated by a spin-on coater to a thickness of about 4,000 to 12,000 Angstroms, having a dielectric constant of less than 2.8 with curing conditions at 400°C for 1 hr., nitrogen ambient gas flow from about 1 to 30 SLM, oxygen less than 10ppm.

3. The method of claim 1, wherein said layer of

adhesion promoter and stabilizer is a non-oxide compound, e.g., silicon nitride deposited by PECVD, plasma enhanced chemical vapor deposition in the thickness range from about 200 to 500 Angstroms.

4. The method of claim 1, wherein said layer of cap oxide or oxide cap is silicon oxide deposited by PECVD, plasma enhanced chemical vapor deposition in the thickness range from about 4,000 to 16,000 Angstroms, having a dielectric constant of about 4.0.

5. The method of claim 5, wherein multilevel metal processing can be performed on the planar surface by repeating the said process steps.

6. A method for fabricating multilevel metal interconnections having low dielectric constant insulators on a substrate comprising the steps of:

providing a semiconductor substrate having semiconductor devices in and on said substrate;

depositing a first insulating layer over said devices, and further having contact openings in said first insulating layer for electrical contacts to said devices;

forming a metal barrier layer on said insulating layer and in said contact openings;

depositing a first conductive layer for contacting said contact openings and forming a metal stack on the interlevel dielectric layer (ILD);

depositing hard mask layer of silicon nitride and then silicon oxide on top of metal layer, with silicon oxynitride DARC, dielectric anti-reflective coating on top of metal stack;

patterning said metal stack consisting of hard mask layer and metal stack layer with said metal barrier layer to form first metal lines as interconnections for said devices;

coating a layer of low dielectric constant insulating material on and in between said patterned interconnect metal lines;

curing the low dielectric constant material;

chemical mechanical polishing (CMP) back and planarizing the surface of said low dielectric constant material with hard mask on top of metal stack;

stopping the CMP polishing on the hard mask layer;

coating the surface with a second layer of low dielectric material;

curing the low dielectric constant material;

depositing a second hard mask layer of silicon nitride and then silicon oxide over the second low dielectric constant layer;

defining via openings and etching for vias to open vias to the underlying interconnect metal;

depositing conductive metal and forming metal contacts by chemical mechanical polishings (CMP) the excess metal, stopping on the polishing on the hard mask layer, thus forming low dielectric constant, low capacitance structures.

7. The method of claim 6, wherein said first hard mask layer is composed of silicon nitride and silicon oxide is deposited by PECVD, plasma enhanced chemical vapor deposition to a thickness of about 200 to 500 Angstroms of silicon nitride and to thickness of about 1,000 to 2,000 Angstroms of silicon oxide.

8. The method of claim 6, wherein said first low dielectric constant material is SOD, spun on dielectric, especially low dielectric organic compounds, and is coated by a spin-on coater to a thickness of about 4,000 to 12,000 Angstroms, having a

dielectric constant of less than 2.8, with curing conditions of 400°C, 1 hr., N_2 gas flow 1 to 30 SLM, O_2 less than 10 ppm.

9. The method of claim 6, wherein said chemical mechanical polishing (CMP) conditions are: polishing rate 1,000 to 2,500 A/min, platen speed of 20 to 80 rpm, carry speed of 20 to 80 rpm, downward force 2 to 8 psi, backside pressure from 1 to 7 psi, polishing back and stopping on the first hard mask.

10. The method of claim 6, wherein said second low dielectric constant material is SOD, spun on dielectric, low dielectric organic compounds especially, and coated by a spin-on coater to a thickness of about 4,000 to 12,000 Angstroms, having a dielectric constant of about of less than 2.8, with curing conditions of 400°C, 1 hr., N_2 gas flow 1 to 30 SLM, O_2 less than 10 ppm.

11. The method of claim 6, wherein said second hard mask layer is composed of silicon nitride and silicon oxide is deposited by PECVD, plasma enhanced chemical vapor deposition to a thickness of about 200

to 500 Angstroms of silicon nitride and to a thickness of about 1,000 to 2,000 Angstroms of silicon oxide.

12. The method of claim 6, wherein said hard mask layers, both first and second hard mask layers can be composed of silicon nitride and silicon oxide, or solely silicon nitride, or solely silicon oxide.

13. The method of claim 6, wherein said chemical mechanical polishing (CMP) conditions are: polishing rate 1,000 to 2,500 A/min, platen speed of 20 to 80 rpm, carry speed of 20 to 80 rpm, downward force 2 to 8 psi, backside pressure from 1 to 7 psi, polishing back and stopping on the second hard mask.

14. The method of claim 6, wherein multilevel metal processing can be performed on the planar surface by repeating the said process steps.

15. A method for fabricating multilevel metal interconnections having low dielectric constant insulators on a substrate comprising the steps of:

providing a semiconductor substrate having semiconductor devices in and on said substrate;

depositing a first insulating layer over said devices, and further having contact openings in said first insulating layer for electrical contacts to said devices;

forming a metal barrier layer on said insulating layer and in said contact openings;

depositing a first conductive layer for contacting said contact openings and forming a metal stack with a silicon oxynitride DARC, dielectric anti-reflective coating, on top of metal, on the interlevel dielectric layer (ILD);

depositing hard mask layer of silicon nitride and then silicon oxide on top of metal layer;

patterning said metal stack consisting of hard mask layer and metal stack layer with said metal barrier layer to form first metal lines as interconnections for said devices;

coating a layer of low dielectric constant insulating material on and in between said patterned interconnect metal lines;

curing the low dielectric constant material;

chemical mechanical polishing (CMP) back and planarizing the surface of said low dielectric constant material with hard mask on top of metal stack;

stopping the CMP polishing on the hard mask layer;

depositing a layer of adhesion promoter over the hard mask and low dielectric constant layer;

depositing a silicon oxide cap layer on the adhesion promoter layer

defining via openings and etching to open electrical contacts to the underlying interconnect metal;

depositing conductive metal over the via openings;

removing the excess said conductive metal by CMP;

patterning of said conductive layer to form the next level of metal interconnections.

16. The method of claim 15, wherein said hard mask layer is composed of silicon nitride and silicon oxide is deposited by PECVD, plasma enhanced chemical vapor deposition, to a thickness of about 200 to 500 Angstroms of silicon nitride and to a thickness of about 1,000 to 2,000 Angstroms of silicon oxide.

17. The method of claim 15, wherein said hard mask layer can be composed of silicon nitride and silicon oxide, or solely silicon nitride, or solely silicon oxide.

18. The method of claim 15, wherein said low dielectric constant material is low dielectric constant SOD, spun on dielectric, low dielectric organic compounds especially, and coated by a spin-on coater to a thickness of about 4,000 to 12,000 Angstroms, having a dielectric constant of about of less than 2.8, with curing conditions of 400°C, 1 hr., N_2 gas flow 1 to 30 SLM, O_2 less than 10 ppm.

19. The method of claim 15, wherein said chemical mechanical polishing (CMP) conditions are: polishing rate 1,000 to 2,500 A/min, platen speed of 20 to 80 rpm, carry speed of 20 to 80 rpm, downward force 2 to 8 psi, backside pressure from 1 to 7 psi, polishing back and stopping on the hard mask.

20. The method of claim 15, wherein said layer of adhesion promoter and stabilizer is silicon nitride deposited by PECVD, plasma enhanced chemical vapor deposition in the thickness range from about 200 to 500 Angstroms, which is deposited on hard mask material.

21. The method of claim 15, wherein said layer of cap oxide is silicon oxide deposited by PECVD, plasma enhanced chemical vapor deposition, in the thickness range from about 4,000 to 12,000 Angstroms, having a dielectric constant of about 4.0, which is deposited on the adhesion promoter.

22. The method of claim 15, wherein multilevel metal processing can be performed on the planar surface repeating the said process steps.

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